WHAT IS CLAIMED IS:

1. An analog multiplier for multiplying a first analog voltage signal at a first frequency by a second analog voltage signal at a second frequency, comprising:

a first stage for converting the first analog voltage signal into a first and a second current signals;

a second stage comprising a first and a second cross-coupled current-switching pairs, driven by the second voltage signal, said first and second current-switching pairs having respective current inputs for receiving the first and the second current signals, respectively;,

parasitic capacitances associated with each of said current inputs of the current-switching pairs; and

a compensation circuit coupled to the current inputs of the current-switching pairs for compensating said parasitic capacitances.

2. The analog multiplier of claim 1, in which an overall impedance of said compensation circuit and of said parasitic capacitances is substantially infinite at said first frequency.

3. The analog multiplier of claim 2, in which said compensation circuit includes a filter designed in such a way to form, together with said parasitic capacitances, a resonating circuit associated with the current inputs of the current-switching pairs and acting a parallel resonator for differential-mode signals at a parallel resonance frequency substantially equal to the first frequency.

4. The analog multiplier of claim 2, in which an overall impedance of said compensation circuit and of said parasitic capacitances is substantially zero at an integer multiple of said second frequency.

5. The analog multiplier of claim 4, in which said filter is further designed in such a way that said resonating circuit acts as a series resonator for common-mode signals at a series resonance frequency substantially equal to an integer multiple of the second frequency.

6. The analog multiplier of claim 5, in which the filter includes a "T"-shaped LC filter, with a first inductive reactance element coupled to a first one of said current inputs, a second inductive reactance element coupled to a second one of said current inputs, and a capacitive reactance element coupled the first and second inductive reactance elements.

7. The analog multiplier of claim 6, in which said first and second inductive reactance elements have a same inductive reactance value designed to make the parallel resonance frequency substantially equal to the first frequency, and the capacitive reactance element has a capacitive reactance value designed to make the series resonance frequency substantially equal to an integer multiple of the second frequency.

8. A method of improving linearity and reducing noise in an analog multiplier including a first stage for converting a first analog voltage signal at a first frequency into a first and a second current signals, and a second stage comprising a first and a second cross-coupled current-switching pairs, driven by a second voltage signal at a second frequency, said first and second current-switching pairs having respective current inputs for receiving the first and the second current signals, respectively, the method comprising:

compensating parasitic capacitances associated with said current inputs of the current-switching pairs.

9. The method of claim 8, in which said compensating comprises

associating with said current inputs a circuit creating parallel resonators resonating at a frequency substantially equal to the first frequency.

10. The method according to claim 9, in which said compensating further comprises associating with said current inputs a circuit creating series resonators resonating at a frequency substantially equal to an integer multiple of the second frequency.

11. A mixer, comprising:

an input stage having an output node and operable to receive an input signal having a first frequency;

an output stage having an input node coupled to the output node and operable to receive a mixing signal having a second frequency; and

a filter coupled to the output node and operable to increase an impedance at the output node at the first frequency and to reduce the impedance at a harmonic of the second frequency.

12. The mixer of claim 11 wherein the input signal comprises a carrier signal having the first frequency and an information signal having a third frequency that is significantly lower than the first frequency.

13. A mixer, comprising:

an input stage having first differential output nodes and operable to receive a differential input signal having a first frequency;

an output stage having first differential input nodes respectively coupled to the differential output nodes and operable to receive a differential mixing signal having a second frequency; and

a filter coupled to the differential output nodes and operable to increase respective impedances at the output nodes at the first frequency and to reduce the impedances at a harmonic of the second frequency.

14. The mixer of claim 13 wherein the input stage comprises:

differential input nodes operable to receive the input signal;

a current source;

a first transistor having a control node coupled to a first one of the differential input nodes, a first current-conducting node coupled to the current source, and a second current-conducting node coupled to a first one of the differential output nodes; and

a second transistor having a control node coupled to a second one of the differential input nodes, a first current-conducting node coupled to the current source, and a second current-conducting node coupled to a second one of the differential output nodes.

15. The mixer of claim 13 wherein the input stage comprises:

differential input nodes operable to receive the input signal;

first and second current sources;

a first transistor having a control node coupled to a first one of the differential input nodes, a first current-conducting node coupled to the first current source, and a second current-conducting node coupled to a first one of the differential output nodes;

a second transistor having a control node coupled to a second one of the differential input nodes, a first current-conducting node coupled to the first current source, and a second current-conducting node coupled to a second one of the differential output nodes;

a third transistor having a control node coupled to the first one of the differential input nodes, a first current-conducting node coupled to the second current source, and a second current-conducting node coupled to the first one of the differential output nodes; and

a fourth transistor having a control node coupled to the second one of the differential input nodes, a first current-conducting node coupled to the second current source, and a second current-conducting node coupled to the second one of the differential output nodes.

16. The mixer of claim 13 wherein the output stage comprises:

second differential input nodes operable to receive the mixing signal;

second differential output nodes;

a first transistor having a control node coupled to a first one of the second differential input nodes, a first current-conducting node coupled to a first one of the first differential input nodes, and a second current-conducting node coupled to a first one of the second differential output nodes;

a second transistor having a control node coupled to a second one of the second differential input nodes, a first current-conducting node coupled to the first one of the first differential input nodes, and a second current-conducting node coupled to a second one of the second differential output nodes;

a third transistor having a control node coupled to the second one of the second differential input nodes, a first current-conducting node coupled to a second one of the first differential input nodes, and a second current-conducting node coupled to the first one of the second differential output nodes; and

a fourth transistor having a control node coupled to the first one of the second differential input nodes, a first current-conducting node coupled to the second one of the first differential input nodes, and a second current-conducting node coupled to the second one of the second differential output nodes.

17. The mixer of claim 13, further comprising:

a reference node; and

wherein the filter comprises,

a first inductive element having a first node coupled to a first one of the first differential output nodes of the input stage and having a second node,

a second inductive element having a first node coupled to a second one of the first differential output nodes and having a second node, and

a capacitive element having a first node coupled to the second nodes of the first and second inductive elements and having a second node coupled to the reference node.

18. The mixer of claim 13, further comprising:

a reference node; and

an inductive element having first and second nodes respectively coupled to the first differential output nodes of the input stage and having a tap, and

a capacitive element having a first node coupled to the tap and having a second node coupled to the reference node.

19. The mixer of claim 13 wherein the harmonic comprises a second harmonic of the second frequency.

20. An electronic system, comprising:

an oscillator operable to generate an oscillator signal;

a mixer, comprising,

an input stage having an output node and operable to receive an input signal having a first frequency,

an output stage having a first input node coupled to the output node, having a second input node coupled to the oscillator, and having an output node, and

a filter coupled to the first input node of the output stage and operable to increase an impedance at the first input node at the first frequency and to reduce the impedance at the second frequency; and

a load coupled to the output node of the output stage.

21. A method, comprising:

mixing a first signal having a first frequency with a second signal having a second frequency to generate a resulting signal having a linearity and a component having a third frequency that is a harmonic of the second frequency;

increasing the linearity with a filter coupled to a node having an impedance; and

attenuating the component with the filter.

22. The method of claim 21 wherein increasing the linearity comprises increasing the impedance at the first frequency.

23. The method of claim 21 wherein attenuating the component comprises decreasing the impedance at the third frequency.